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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/814,355	03/21/2001	Robert Warren Sherburne JR.		3657

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/814,355	SHERBURNE, ROBERT WARRE	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 21-39 are presented for examination. Claims 1-20 are canceled.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/27/04 has been entered.

Terminal Disclaimer

4. The terminal disclaimer filed on 12/27/04 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. application no. 09/837,651 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Specification

5. The disclosure is objected to because of the following informalities: on page 12, line 4, "processor 310" should be -- processor 320 --(see figure 2); on page 12, line 5, "buffer 318" should be -- buffer 324 --(see figure 2). Appropriate correction is required.

Drawings

6. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because number and reference characters not plain and legible in figures 1-6. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

7. Claim 24 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to disclose that the first processor unit and the second processor unit comprise a reconfigurable processor core. As shown in figure 5 and in specification pages 17-18, **ONLY** a reconfigurable processor core 150 comprises one or more processors.

For examination purpose, the examiner examines the claim 24 as "a reconfigurable processor core comprises the first processor unit and the second processor unit". Applicant is welcome to provide feed back in next response to clarify the issue.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 30, 32 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Gulick (Gulick), US patent no. 5,778,218.

Gulick is the references cited in prior office action.

As per claim 30, Gulick discloses a system [fig. 4] comprising:

a first processor [DSP 2028, fig. 5] to receive a first clock signal to control performance of the firs processor [col. 6, lines 44-46];

a first buffer coupled to an output of the first processor [2018, fig. 5; col. 6, lines 14-16] ; and

a first controller to generate the first clock signal from a master clock, the first controller to receive a first feedback signal from the first buffer and to control the first clock signal based on the first feedback signal to optimize processing power of the first processor [col. 6, lines 49-63; col. 7, lines 23-52].

As per claim 32, Gulick discloses that the first controller to provide a write signal to the first buffer based on the first feedback signal [fig. 5; col. 7, lines 24-60].

As per claim 33, Gulick discloses that the first controller to lower a frequency of the first clock signal if the first feedback signal is above a threshold [col. 7, lines 24-60].

10. Claims 21-22, 24-26, 28, 29, 31 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick (Gulick), US patent no. 5,778,218 in view of Ohmori (Ohmori), US patent no. 6,647,502.

Gulick and Ohmori are the references cited in prior office action.

As per claim 21, Gulick discloses an integrated circuit [fig. 5] comprising:

a first processor unit [DSP 2028, fig. 5] to receive a first clock to control performance of the first processor unit [col. 6, lines 44-46];

a first buffer [2018, fig. 5; col. 6, lines 14-16] coupled to an output of the first processor unit, the first buffer clocked by a master clock [PC's clock 2003; col. 7, lines 15-17];

a second processor unit [CPU 2002, fig. 5] to receive a second clock to control performance of the second processor unit [col. 5, line 66-col. 6, line 2]; and

at least one clock controller to generate the first clock, and to vary a frequency of the first clock [fig. 5; col. 6, lines 49-63; col. 7, lines 53-63].

Gulick does not explicitly disclose that at least one controller generate the second clock, and to vary a frequency of the second clock.

Ohmori discloses that at least one controller generate the second clock, and to vary a frequency of the second clock [col. 3, line 64-col. 4, line 4; col. 9, lines 33-35, 44-47].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Gulick and Ohmori because they are both directed to vary clock frequency according to data level of the buffer, and the specify teachings of Ohmori stated above would have allowed for greater processing efficiency by adjusting the second clock frequency for the second processor.

As per claim 22, Gulick discloses that a memory coupled to the first processor unit and the second processor unit [figures 4, 5].

As per claim 24, Ohmori discloses that a reconfigurable processor core comprises the first processor unit and the second processor unit [fig. 1; col. 4, lines 46-48; col. 8, lines 34-36].

As per claim 25, Gulick discloses that the first buffer to provide a feedback signal to the at least one clock controller, the at least one clock controller to vary the first clock based on the feedback signal [col. 6, lines 55-63; col. 7, lines 43-52]. Ohmori discloses that the first buffer to provide a feedback signal to the at least one clock controller, the at least one clock controller to vary the first clock based on the feedback signal [col. 3, line 64-col. 4, line 4; col. 9, lines 33-35, 44-47].

As per claim 26, Gulick discloses that the first clock is different than the master clock [fig. 5; col. 6, lines 45-50; col. 7, lines 15-17].

As per claim 28, Gulick discloses that the first processor unit comprises a digital signal processor (DSP) [fig. 5; col. 6, lines 44-45].

As per claim 29, Ohmori discloses that the frequency is varied to optimize speed and processing power for a task [col. 3, line 64-col. 4, line 4; col. 7, lines 44-54; col. 9, lines 19-47].

As per claim 31, Ohmori discloses a second processor coupled to an output of the first buffer to receive a second clock signal to control performance of the second processor [col. 3, line 64-col. 4, line 4; col. 7, lines 44-54; col. 9, lines 19-47].

11. Claims 23, 34, 35 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick (Gulick), US patent no. 5,778,218 in view of Ohmori (Ohmori), US patent no. 6,647,502 and Yano et al. (Yano), US patent no. 6,807,235.

As to claim 23 and 34, Gulick and Ohmori do not disclose a wireless transceiver.

Yano discloses a wireless transceiver coupled to the first processor unit and the second processor unit [figures 2, 3; col. 3, lines 55-62].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Gulick and Ohmori and Yano because they are directed to data processing system, and the specify teachings of Yano stated above would have allowed for greater functionality by using wireless data transfer and utilizing Gulick's system in wireless system.

As per claim 35, inherently, Yano discloses an input sensor coupled to the first processor to receive visual information [figures 1, 2; col. 3, line 54-col. 4, line 6].

12. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick (Gulick), US patent no. 5,778,218 in view of Ohmori (Ohmori) US patent no. 6,647,502 and Nishiyama et al. (Nishiyama), US Patent no. 5,790,877.

Nishiyama is the references cited in prior office action.

As per claim 27, Gulick and Ohmori fail to explicitly disclose the first processor unit includes a reduced instruction set computer (RISC) processor.

Nishiyama discloses the first processor unit comprises a RISC processor [col. 3, lines 35-42].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Gulick and Ohmori and Nishiyama because they are directed to a processor core, and the specify teachings of Nishiyama stated above would have allowed for greater processing capabilities by using the RISC processor to improve the functionality of Gulick's system.

13. As to claims 36-39, claims 21-26 basically are the corresponding elements that are carried out the method of operating steps in claims 36-39. Accordingly, claims 36-39 are rejected for the same reason as set forth for claims 21-26.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

Mar. 2, 2005